ATTORNEY DOCKET NO. : MERCHANT 33-3-3 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Sailesh Merchant, *et. al.*

Serial No.: 09/092,158

Filed: June 6, 1998

For: METHOD FOR THE FABRICATION OF CONTACTS IN AN INTEGRATED CIRCUIT DEVICE

Grp./A.U.: 2823

Examiner: Eaton, K.

Commissioner of Patents
and Trademarks
Washington, D. C. 20231

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 3/29/01 (Date)
GLENDA L. WILLIS Printed or typed name of person signing the certificate
Glenda L. Willis
(Signature of the person signing the certificate)

Sir:

AFFIDAVIT UNDER 37 C.F.R. §1.131

State of New Jersey §
§
§
County of Essex §

Sailesh Merchant, being duly sworn, deposes and states:

1. I am a joint inventor of claims 1, 2, 4-12 and 14-24 of the patent application identified above and a joint inventor of the subject matter described and claimed therein.

2. Prior to March 24, 1998, I conceived and reduced to practice a method of fabricating contacts in an integrated circuit device as covered by the above-identified patent application, as

evidenced by the following:

a. I entered the notations of my conception and reduced the invention to practice prior to March 24, 1998. These notations are reflected on the Patent Committee Invention Submission form which is kept in the regular course of business for formally commemorating the conception and reduction to practice of inventions (see copy attached hereto as Exhibit A).

b. The dates omitted from Exhibit A are prior to March 24, 1998.

Sailesh Merchant

Sworn to and subscribed before me this 22nd day of March, 2001.

ELLIE ROBERTS
MY COMMISSION EXPIRES
September 29, 2003
#CC 871149
Bonded thru
Notary Public Underwriters
NOTARY PUBLIC, STATE OF FLORIDA

Notary Public

APR 0 2 2001

MICROELECTR[redacted] PATENT COMMITTEE INV[redacted] SUBMISSION

PROCESSING

Name(s) of Submitters	Telephone No	Loc/Room	Organization	E-mail Address
S.M. Merchant	407-345-7538	301C2100	538114000	smerchant@lucent.com
M. Oh	407-345-7638	301C2102	538114000	minseokoh@lucent.com
B. Nguyenphu	407-345-6747	301C2150	55K11E000	orbnp@micro.lucent.com

IP LAW USE

Submission No 113941

Date Received

Attorney: Q.T. Dinh

Title: A NOVEL METHOD FOR THE FABRICATION OF W-PLUGS

Problem(s) addressed by the invention: Ti/TiN films are commonly used as an adhesion/barrier underlayer for W-plugs in CMOS and bipolar technologies. With large aspect ratio windows, thicker TiN films (≥750A) are required for defect-free and volcano-free W deposition. Moreover, for improved contact resistance, enhanced Ti/TiN bottom coverage is achieved using collimation techniques during PVD deposition. Increased intrinsic stress attendant with thicker TiN films, especially when the TiN is deposited at lower temperatures or is collimated, causes these films to crack after barrier and junction anneals, such as when using an RTA. In the worst case, high stresses can cause stack delamination, lack of W-plug adhesion and ultimately device failure. The present invention prevents such TiN cracking and lifting with the use of a novel W-plug fabrication technique.

Closest known solution: Use of low-stress TiN films such as plasma-treated CVD TiN that is costly and has low throughput over conventional PVD or collimated TiN.

DESCRIPTION OF THE INVENTION, keyed to drawings, sketches, photographs, etc., sufficient to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention.

Summary (30 words or less): Use of an novel processing sequence, specifically the position of the barrier anneal RTA during W-plug formation sequence, prevents TiN films from cracking and delamination caused by high stresses.

Detailed Description: A conventional processing sequence for W-plug fabrication at the contact level (window) is as follows: PVD Ti/TiN deposition + RTA + CVD-W deposition + W/TiN/Ti-CMP + Interconnect deposition. Such a sequence frequently leads to cracking of the TiN, especially in the field areas where the TiN layer is thick. The proposed invention follows the following sequence: PVD Ti/TiN deposition + CVD-W deposition + W/TiN/Ti-CMP + RTA + Interconnect deposition. In the proposed sequence, the TiN does not get annealed before the W-plug is deposited and hence cracking is avoided. When the W/TiN/Ti stack is polished using CMP, the only TiN left behind on the wafer is that in the W-plugged contacts. This TiN is very thin, approximately 5-20% of the original field thickness. Since this is only a fraction of the field thickness, when such a thin TiN film is annealed using an RTA, after the W-plug is formed, no evidence of cracking is seen in the contacts. Thus a defect-free W-plug is obtained.

Advantages: A defect-free W-plug module without cracked adhesion/barrier layers.

Commercial product(s) or other application in which the invention may be used: All sub-0.25 um products using our core CMOS and Bi-CMOS technologies and their enhancement modules.

** Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc.***

Submitter(s) signature(s) and date

	date		date
	date		date
	date		date

This invention submission has been read and understood by the following two witnesses:

	date		date
	date		date